Docket No. MTI-31267

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant (s)	:	Polinsky, William, et al.
Serial No.	:	09/854,975
For	:	Modified Facet Etch to Prevent Blown Gate Oxide and Increase Etch Chamber Life
Filed	:	May 14, 2001
Examiner	:	Lynette T. Umez Eronini
Group Art Unit	:	1765
Confirmation No.	:	9089

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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37 CFR 1.8(a)

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Dear Sirs:

APPEAL BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from the final rejection of Claims 1-21 as stated in the Office Action mailed May 6, 2003. The Notice of Appeal was timely filed on October 8, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technologies, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related applications currently either under appeal or the subject of an interference proceeding.

III. STATUS OF CLAIMS

All the claims of this application and their individual status are reported in Appendix 1 to this Appeal Brief. Claims 1-21 are on appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF INVENTION

The current invention is a method of facet etching of a semiconductor device by two sequential etching steps. The first step etches the device with a high energy plasma beam. The first etch is terminated at a predetermined depth that is less than the target depth for the entire etching process. The second step uses a reactive chemical gas/plasma to finish the etch to the target depth. Advantages of this inventive two-step etch include, *inter alia*, both decreased possibility of etching through the gate oxide and also self-cleaning of the etching chamber.

The invention is described in more detail in the specification. A description of typical semiconductor devices useful in the practice of this invention is given from page 3, line 19 through page 4, line 20. The first step high energy plasma facet etch is described from page 4, line 21 through page 6, line 4. The second step chemical gas/plasma etch is described from page 6, lines 5 through 9.

VI. ISSUES

The issue on appeal is whether or not the following final rejections are in error:

The Examiner finally rejected Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention.

The Examiner finally rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Doan (USP 5,346,585) in view of Laxman (USP 5,774,196) in view of Yao, et al.. (USP 5,814,564).

The Examiner finally rejected Claims 11-21 under 35 U.S.C. § 103(a) as being unpatentable over Doan in view of Laxman and Yao, et al.. and further in view of Lee (USP 5,935,875).

VII. GROUPING OF CLAIMS

In the arguments below, Claims 1-10 stand together and Claims 11-21 stand together.

VIII. ARGUMENT

ERROR 1: The rejection of Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. §112, second paragraph fails to properly consider standard terminology in the art and is therefore in error.

The Examiner rejected some of the claims as being indefinite. The Appellants believe that the fundamental error of this rejection is the Examiner's failure to understand and consider standard usage of terms in the art and in patent claims. Specifically, the Examiner ignores thousands of examples demonstrating the correctness of the terms used in the appealed claims.

A. Requirements For A Rejection Under 35 U.S.C. §112, Second Paragraph

The definiteness inquiry focuses on whether those skilled in the art would understand the scope of the claim when the claim is read in light of the rest of the specification. *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986); *Seattle Box Co. v. Industrial Crating & Packing Inc .*, 731 F.2d 818, 826, 221 USPQ 568, 574 (Fed. Cir. 1984); *In re Morasi*, 710 F.2d 799, 803, 218 USPQ 289, 292 (Fed. Cir. 1983). Even if

the written description does not enable the claims, the claim language itself may still be definite. *In re Hyatt*, 708 F.2d 712, 714-15, 218 USPQ 195, 197 (Fed. Cir. 1983); *In re Miller*, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971) ("[B]readth is not to be equated with indefiniteness ....").

B. The Final Rejection

The Examiner finally rejected Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention. Specifically, the Examiner finds the meaning of the term "target depth" unclear. Additionally, the Examiner finds the term "predetermined" indefinite because it reads on a nebulous metal step conducted prior to manipulative steps of the claimed invention. In response to the Appellants well-supported arguments that both "predetermined depth" and "target depth" are standard terms in the art the Examiner raises two points: (1) that the terms fail to define over a generic depth and (2) that claim 9 of USP 6,511,777 defines the predetermined depth specifically.

C. Reasons the Rejection is in Error

The Final Rejection fails to address and meet the standard for a rejection for indefiniteness and also ignores the mass of evidence supporting the validity of the claims. As argued below, both "target" depth and "predetermined" depth are standard terms and which one skilled in the art would clearly understand, especially viewed in light of the specification.

For example, the term "target depth" is clear from the claims, is fully described in the specification and is a standard term of art. The claims clearly state that target depth is the depth at which the inventive etching process is terminated. See preamble to Claim 1 and final step of each independent claim. Additionally, the term is used unambiguously to mean such throughout the specification. Moreover, the term "target depth" is a term of art found in the granted claims of other U.S. patents which are, of course, presumed to be valid with respect to all sections of the statute. Likewise, the term "predetermined depth" is a standard term found in numerous U.S. patents.

Indeed, over 3600 U.S. patents use one or the other of these terms in their claims. See attached cover sheet of a search result on the USPTO database. (Appendix 2). Although, the Appellant has not reviewed all of these U.S. patents, a random sampling indicates that the Appellant has used standard terms in their standard usage. See, e.g., the claims pages for USP Nos., 586,702; 6,583,054; 6,518,624 and 6,511,777 which demonstrate the use of the term "predetermined depth" in a manner identical to the current claims; see also, e.g., the claims page of USP No. 6,225,234 which uses the term "target depth" in a manner identical to the manner of the appealed claims. (Appendix 3).

The two points that the Examiner raised in the response to Appellants arguments are also in error.

There are at least two reasons why the Examiner's first point is in error. First, as argued above, the terms in dispute are standard terms of art which must relate to a specific depth that is understood by one skilled in the art. As such, the use of these terms to identify a certain depth must, by definition, be different than a generic depth or else the at least 3600 persons skilled in the art (as represented by the issued U.S. patents) would not have used the terms. Second, the Examiner is completely discounting the ability of those skilled in this art. Such a skilled person would not be etching the substrate unless the design and production process of the semiconductor chip requires such etching. Such design and process considerations would also include the target depth to which the etch is conducted. In other words, one skilled in the art would not begin an etching process unless that person knew when to terminate the etch. Determination of the target depth is not the subject of the current claims, but rather, the subject is a method facet etching to a predetermined depth. As such, one skilled in the art would recognize that determining the absolute magnitude of the predetermined target depth was merely a design consideration of the chip being manufactured and not part of the current invention. Therefore, the specification, e.g., page 5, line 21 through page 6, line 4, FIG. 4 and FIG. 5, fully enables and supports the terminology of the current claims.

The Examiner's second point is also clearly in conflict with U.S. patent laws. Specifically, claim 9 of the US'777 patent that the Examiner cites is merely a dependent claim that further defines and limits the term "predetermined depth". Apparently, the Examiner is

either reading the limitations of dependent claim 9 into the claims it depends from (all of which use the term "predetermined depth" without further description) or is assuming that those preceding claims are all invalid. As the Examiner is aware, all claims of a U.S. patent are presumed to be valid. Additionally, the Examiner is surely aware that limitations from dependent claims are not to be read into the independent claims. As such, even in the patent that the Examiner cites, the term "predetermined depth" is used in at least Claims 1-8, without additional description. Moreover, the Examiner's contention, even if it were correct (which the Appellant denies), only addresses one patent, not the entire list of support that the Appellant cites.

In addition, a number of courts, including the Federal Circuit, have passed judgment on the validity, under 35 U.S.C. §112, of claims which contain the term "predetermined" as used in the current claims under appeal. These courts did not even find it necessary to comment on whether the term "predetermined" renders a claim indefinite, much less hold against the validity of a claim on that ground. See, e.g., *All Dental Prodx LLC v. Advantage Dental Products Inc.*, 64 USPQ2d 1945 (Fed. Cir. 2002); *Bose Corp. v. JBL Inc.*, 61 USPQ2d 1216 (Fed. Cir. 2001).

In summary, the evidence clearly shows that both federal courts and those skilled in the art are able to understand the scope and meaning of a claim that contains either "target" or "predetermined". Thus, the rejection under 35 U.S.C. §112, second paragraph, fails and must be overturned.

The Examiner also rejected the claims as obvious over various combinations of references. The Appellants believe that the fundamental errors in the Examiner's *prima facie* cases are that the proposed combinations of references are not permitted under current U.S. patent law. Specifically, the Examiner's proposed combinations and modifications improperly change the principle of operation of at least one reference and make the inventions of the references unsuitable for their original purposes.

ERROR 2: The rejection of Claims 1-10 under 35 U.S.C. §103(a) is in error because the proposed *prima facie* case is insufficient and also legally barred.

The Appellants believe that the Examiner has failed to meet the standards for an obviousness rejection and, therefore, has not established a *prima facie* case of obviousness.

A. Requirements for a *Prima facie* Case of Obviousness

The Examiner's fundamental error in rejecting the claims on appeal is that he has failed to establish a *prima facie* case of obviousness.

> In rejecting claims under 35 U.S.C. §103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness . . . 'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art . . .'" *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993).

Specifically, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. See *In re Royka*, 180 USPQ 580 (CCPA 1974). In addition, in order to establish a *prima facie* case of obviousness, the Examiner must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. *See, e.g., In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Furthermore, in leading one skilled in the art, the prior art must suggest to the ordinary skilled artisan that the combination should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. *In re Dow Chemical Co*, 5 USPQ2d 1529, 1532 (Fed. Cir. 1988)(emphasis added). Indeed, both the suggestion and the expectation of success must be found in the prior art, not in the Appellant's disclosure. Id. Additionally, the Federal Circuit has stated that a reference should be considered in its entirety, with due consideration given to disclosures that diverge or teach away from the invention as well as disclosures which direct one skilled in the art to the invention. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 669 (Fed. Cir. 1985).

Furthermore, certain combinations or types of modifications of the prior art are legally barred to prevent the USPTO from applying improper hindsight to the obviousness

determination. Relevant here, if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Equally relevant, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

B. Final Rejection

The Examiner finally rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Doan (USP 5,346,585) in view of Laxman (USP 5,774,196) in view of Yao, et al.. (USP 5,814,564). The Examiner states that Doan teaches a method for facet etching a semiconductor device to a target depth. The Examiner admits that Doan fails to teach both that the first layer is formed to a thickness at least equal to the target depth and that the specified depth in which the first etch is terminated with respect to the target depth. The Examiner then relies on Laxman to demonstrate that the layer thickness is a results effective variable. The Examiner then also admits that Doan in view of Laxman fails to teach: terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth; etching the first layer in a second etch by contacting the first layer with a reactive chemical gas/plasma; and terminating the second etch when the first layer has been etched to the target depth. The Examiner then relies on Yao, et al.. for the teaching of a method of etching back an oxide layer by employing six etching steps. The Examiner states that "since each of these steps are performed in a specified time, then using Yao, et al..'s steps of etching an oxide layer would inherently read on [the current claims]".

C. Reasons the Rejection is in Error

The Appellants believe that the Examiner's § 103 rejections fail to meet the above standards. Furthermore, the Examiner has failed to address the prior contentions that the Examiner's proposed combination of references is legally barred. Specifically, the Examiner has not responded to the arguments that Yao teaches away from the current invention because the

unexpected results reported by Yao are stated to be due to the specific sequential steps. Likewise, the Examiner has not responded to the arguments that the combination with Yao is legally barred because such a combination would change the principle of operation of Yao. Therefore, the following legal arguments stand uncontradicted.

First, as the Examiner has stated, Doan teaches facet etching a semiconductor device to a target depth. Thus, Doan does not teach terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth. There is no disclosure or suggestion in Doan of terminating the etch prior to the target depth or using a two-stage etch. Indeed, for the purposes of Doan, terminating the facet edge prior to reaching the target depth would be unsuitable because the target depth would not then be reached. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Moreover, a two stage etch, wherein the second stage etch is done by contacting the first layer with a reactive chemical gas/plasma, is a different principle of operation from a one stage etch performed exclusively with a plasma beam as taught in Doan. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). As such, Doan fails to teach or suggest the current invention and may not be properly modified as proposed by the Examiner.

The Examiner's use of Laxman does not advance the proposed *prima facie* case. Indeed, the teaching of Laxman is irrelevant to the current invention. The teaching of Laxman, at best, may be interpreted to indicate that layer thickness is a result effective variable in some context but the teaching does not indicate that layer thickness is a result effective variable in the context of the current method of facet etching. While the thickness of an insulating layer may well affect the performance of a semiconductor device, the layer thickness does not affect the performance of the current method. In other words, one skilled in the art would not change the thickness of a layer expecting to improve or alter the performance of the current method. Rather, the operational parameters of the current method would be optimized for different layer thicknesses.

Moreover, even if Laxman did render the thickness of the first layer obvious (which the Appellant strongly denies) it adds no teaching whatsoever regarding the relationship between the thickness of the first layer and the target depth.

The combination of Yao, et al.. and the combined teachings of Doan and Laxman is neither proper nor provides the missing teachings. The Examiner states that the six step etch of Yao, et al.. inherently covers the current claims. However, the Appellants believe that the Examiner has failed to meet the stringent requirements of an obviousness rejection based upon inherency.

In order to establish a *prima facie* case of obviousness based on inherent properties, the Examiner must show that the undisclosed properties are not only inevitably and necessarily present, but also that the inherency of the undisclosed properties or elements is obvious to one skilled in the art. *Kloster Speedsteel AB v. Crucible Inc.,* 230 USPQ 81, 88 (Fed. Cir. 1986). However, the Examiner has not shown, no is there, any teaching or suggestion in Yao, et al.. which would obviously indicate to one skilled in the art that the two step etch of the current claims is necessarily and inevitably the result of the teaching of Yao, et al.. As such, the Examiner has not met the burden necessary for basing an obviousness rejection on an inherent property.

Moreover, not only does Yao, et al.. not inherently cover the current claims, Yao, et al.. explicitly teaches away from the methods of the current claims. Yao, et al.. state that their unexpected results are due to the specific combination of steps 2-5. See column 3, lines 1-10. However, the sequential steps of Yao, et al.. are in reverse order to the steps of the current method. In other words, Yao, et al.. teaches away from the claimed sequence of steps. The Appellants also point to the following differences between Yao, et al.. and the current claims.

Furthermore, Yao, et al.. performs chemical etching prior to plasma etching. This is a different principle of operation than the current claims. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Moreover, the goal of Yao, et al.. is to obtain a highly smooth planarized surface. Modifying the teachings of Yao, et al.. to do a facet etch would render the surface distinctly non-planar and as such, would be unusable for the purpose of Yao, et al.. In addition, Steps 3-6 of Yao, et al.. etches the semiconductor device beyond the first layer. This means that the target depth of the etch of Yao, et al.. is greater than the depth of the first layer contrary to the language of the current claims. For the above reasons, even if, arguendo, Yao, et al.. were properly combinable with Doan in view of Laxman, such a combination fails to teach the steps of the current method claim.

For any and all of the reasons set forth above, the rejections of Claims 1-10 under § 103(a) fail to meet the legal requirements of a *prima facie* case of obviousness and must, therefore, be overturned.

ERROR 3: The rejection of Claims 11-21 under 35 U.S.C. §103(a) is in error because the proposed *prima facie* case is insufficient and also legally barred.

A. Requirement of a Prima Facie Case of Obviousness

As above for ERROR 2.

B. The Final Rejection

The Examiner finally rejected Claims 11-21 under 35 U.S.C. § 103(a) as being unpatentable over Doan in view of Laxman and Yao, et al.. and further in view of Lee (USP 5,935,875). The combination of Doan in view of Laxman and Yao, et al.. is used as above for the rejections of Claims 1-10. The Examiner states that Doan in view of Laxman and Yao fail to teach forming a second layer comprising an insulating material superjacent the first layer. The Examiner cites Lee for the teaching of forming a second insulating layer over a first insulating layer and concludes that it would be obvious for one skilled in the art to modify Doan in view of Laxman and Yao by using Lee's method.

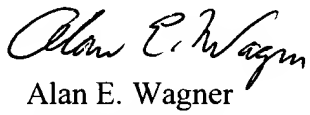
C. Reasons the Rejection is in Error

This rejection suffers from the same deficiencies as the rejection in ERROR 2. As argued above, the combination of Doan in view of Laxman in view of Yao, et al.. is not proper and also fails to disclose the elements of the current claims. The above arguments from ERROR 2 are repeated herein by reference. The addition of Lee does not remedy the deficiencies in the combined teachings of Doan in view of Laxman and Yao, et al.. nor does it render such a combination proper. As such, this rejection is improper and the *prima facie* case fails.

IX. REQUEST

For the reasons stated in the above argument, Appellants believe that the claims on appeal comply with 35 U.S.C. §103(a), and they request that the final rejection of the claims on appeal be reversed.

Respectfully submitted,



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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330

Complete if Known	
Application Number	09/854,975
Filing Date	May 14, 2001
First Named Inventor	Polinsky, et al.
Examiner Name	L. T. Ulrey Eromini
Art Unit	1765
Attorney Docket No.	MTI-31267

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X =
Independent Claims		- 3** =		X =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	(330)	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	ALAN E. WAGNER	Registration No. *(Attorney/Agent)*	45188	Telephone	414-273-2100
Signature	Alan E. Wagner			Date	12/8/03

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APPENDIX 1

The claims on appeal are:

WHAT IS CLAIMED IS:

1. A method for facet etching a semiconductor device to a target depth, the method comprising the steps of:

forming a first layer comprising an insulating material superjacent a substrate comprising a plurality of conductive structures, at least some of the conductive structures being placed apart to form spaces between the conductive structures, such that the first layer forms in at least some of the spaces between the conductive structures and the first layer is formed to a thickness at least equal to the target depth;

etching the first layer, in a first etch, by directing a plasma beam at the first layer formed in at least some of the spaces between the conductive structures, wherein the plasma is of sufficient energy to sputter material from the first layer and the plasma is an ion of an inert gas thereby forming a facet etch in the first layer formed in the spaces between the conductive structures;

terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth;

etching the first layer, in a second etch, by contacting the first layer with a reactive chemical gas/plasma; and

terminating the second etch when the first layer has been etched to the target depth.

2. The method of Claim 1 wherein the first layer is formed by means of chemical vapor deposition.
3. The method of Claim 1 wherein the first layer comprises silicon dioxide or boron phosphosilicate glass.

4. The method of Claim 1 wherein the conductive structures form at least one of metal lines, interconnects and leads.
5. The method of Claim 4 wherein the conductive structures comprise at least one of titanium, tungsten, tantalum, molybdenum, aluminum, copper, gold, silver, nitrides thereof and silicides thereof.
6. The method of Claim 1 wherein the inert gas is at least one of helium, argon, xenon, krypton.
7. The method of Claim 1 wherein the plasma has an energy of about 300 to about 700 W.
8. The method of Claim 1, wherein the first etch is terminated at a depth no more than about 150 Å less than the target depth.
9. The method of Claim 1, wherein the first etch is terminated at a depth no more than about 100 Å less than the target depth.
10. The method of Claim 1 wherein the first etch is terminated at a depth about 50 Å less than the target depth.
11. A method for improving dielectric step coverage, the method comprising the following steps:

forming a first layer comprising an insulating material superjacent a substrate comprising a plurality of conductive structures, at least some of the conductive structures being placed apart to form spaces between the conductive structures, such that the first layer forms in at least some of the spaces between the conductive structures and the first layer is formed to a thickness at least equal to the target depth;

etching the first layer, in a first etch, by directing a plasma at the first layer formed in at least some of the spaces between the conductive structures, wherein the plasma is of sufficient energy to sputter material from the first layer and the plasma is an ion of an inert gas thereby forming a facet etch in the first layer formed in the spaces between the conductive structures;

terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth;

etching the first layer, in a second etch, by contacting the first layer with a reactive chemical gas/plasma;

terminating the second etch when the first layer has been etched to the target depth, and

forming a second layer comprising an insulating material superjacent the first layer.

12. The method of Claim 11 wherein the second layer uniformly covers the first layer.

13. The method of Claim 11 wherein the first layer is formed by means of chemical vapor deposition.

14. The method of Claim 11 wherein the first layer comprises silicon dioxide or boron phosphosilicate glass.

15. The method of Claim11 wherein the conductive structures form at least one of metal lines, runners, interconnects and leads.

16. The method of Claim 15 wherein the conductive structures comprise at least one of titanium, tungsten, tantalum, molybdenum, aluminum, copper, gold, silver, nitrides thereof and silicides thereof.

17. The method of Claim11 wherein the inert gas is at least one of helium, argon, xenon, krypton.

18. The method of Claim 11 wherein the plasma has an energy of about 300 to about 700 W.

19. The method of Claim 11 wherein the first etch is terminated at a depth no more than 150 Å less than the target depth.

20. The method of Claim 11 wherein the first etch is terminated at a depth no more than 100 Å less than the target depth.

21. The method of Claim 11 wherein the first etch is terminated at a depth about 50 Å less than the target depth.

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ACLM/"predetermined depth" OR ACLM/"target depth": 3639 patents.
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Next 50 Hits

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Refine Search ACLM/"predetermined depth" OR ACLM/"target depth

	PAT. NO.	Title
1	6,586,702	High density pixel array and laser micro-milling method for fabricating array
2	6,584,751	High speed machine for inserting sheets into envelopes
3	6,583,381	Apparatus for fabrication of miniature structures
4	6,583,054	Method for forming conductive line in semiconductor device
5	6,583,032	Method for manufacturing semiconductor chips
6	6,582,445	Trephine for lamellar keratectomy
7	6,579,282	Device and method for creating a corneal reference for an eyetracker
8	6,578,321	Embeddable mounting device
9	6,577,051	Flat cathode ray tube
10	6,576,407	Method of improving astigmatism of a photoresist layer
11	6,575,882	Exercise device having weights and safety mechanism to maintain weights in place
12	6,575,712	Air compressor system
13	6,575,436	Evaporative cooler
14	6,575,313	Structure for firmly resting tools thereon
15	6,575,192	Check valve for a prechamber assembly
16	6,574,984	Refrigerator door mounted water dispensing assembly
17	6,574,494	Methods, systems and computer program products for photogrammetric sensor position estimation
18	6,574,433	Underwater camera housing
19	6,573,583	Semiconductor device and method of manufacturing the same
20	6,573,136	Isolating a vertical gate contact structure

United States Patent **6,583,054**
Kwon **June 24, 2003**

Method for forming conductive line in semiconductor device

Abstract

Provided with a method for forming conductive lines in a semiconductor device including the steps of: (a) forming a first conductive line on a substrate; (b) forming a first insulating layer on the substrate as well as on the first conductive line; (c) etching the first insulating layer on the first conductive line to form a first opening; (d) forming a second insulating layer on the first insulating layer to be in contact with the upper part of the first opening, thereby sealing the first opening; (e) etching the first and second insulating layers corresponding to the first conductive line to form a second opening and at the same time extend the first opening so as to expose the first conductive line; and (f) forming a second conductive line within the first and second openings so as to be connected with the first conductive line, thereby preventing halation caused by irregular reflection during exposure on the second photo resist because the second insulating layer has a less difference in thickness, and suppressing decrease in the exposed area of the first conductive line caused by extension of the first opening.

Inventors: **Kwon; Tae-Seok** (Chungcheongbuk-do, KR)
Assignee: **Hyundai Microelectronics Co., Ltd.** (Chungcheongbuk-do, KR)
Appl. No.: **421092**
Filed: **October 19, 1999**

Foreign Application Priority Data

Feb 22, 1999[KR] 1999-5794

Current U.S. Class: **438/638**; 438/624; 438/627; 438/706; 438/786
Intern'l Class: H01L 021/476.3; H01L 021/302; H01L 021/469
Field of Search: 438/622-624,627,629,631,633,637-640,700,706,786,791

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Primary Examiner: Nguyen; Ha Tran
Attorney, Agent or Firm: Morgan, Lewis & Bockius LLP

Claims

What is claimed is:

1. A method for forming conductive lines in a semiconductor device comprising the steps of:

(a) forming a first conductive line on a substrate;

(b) forming a first single insulating layer on the substrate as well as on the first conductive line;

(c) etching the first single insulating layer on the first conductive line to form a first opening;

(d) forming a second insulating layer on the first single insulating layer to be in contact with the upper part of the first opening, thereby sealing the first opening and defining a void at a lower part of the first opening;

(e) etching the first single and second insulating layers corresponding to the first conductive line to form a second opening and at the same time extend the first opening so as to expose the first conductive line; and

(f) forming a second conductive line within the first and second openings so as to be connected with the first conductive line.

2. The method as claimed in claim 1, wherein the step (c) of forming the first opening comprises the steps of:

forming a first photo resist on the first single insulating layer to expose a portion corresponding to a portion of the first conductive line; and

etching the first single insulating layer as deep as a ***predetermined depth*** by using the first photo resist as a mask.

3. The method as claimed in claim 1, wherein the second insulating layer is deposited to have overhangs occurring at the upper edge of the first opening and being in contact with one another to seal the first opening.

4. The method as claimed in claim 3, wherein the second insulating layer is formed by a plasma enhanced chemical vapor deposition using SiH.sub.4 or TEOS (tetraethyl orthosilicate) as a reactive gas, or by a sputtering method.

5. The method as claimed in claim 1, wherein the step (e) of forming the second opening comprises the steps of:

forming a second photo resist on the second insulating layer so as to expose a portion including a portion corresponding to the first opening; and

etching the first single and second insulating layers by using the second photo resist as a mask.

6. The method as claimed in claim 5, wherein the second opening is wider than the first opening.

7. The method as claimed in claim 1, wherein the step (f) of forming the second conductive line comprises the steps of:

depositing the second conductive line on the second insulating layer to fill the first and second openings; and

performing an etch back upon the second conductive line so as to expose the second insulating layer.

8. The method as claimed in claim 7, further comprising the steps of removing the second insulating layer.

9. The method as claimed in claim 1, further comprising the steps of forming a barrier metal layer on the surface of the first and second openings.

10. The method as claimed in claim 9, wherein the barrier metal layer is formed by continuously depositing titanium (Ti) and titanium nitride (TiN) by a sputtering method.

11. The method as claimed in claim 9, wherein the step (f) of forming the second conductive line comprises the steps of:

depositing a conductive material on the barrier metal layer to fill the first and second openings; and

performing an etch back upon the conductive material and the barrier metal layer so as to expose the second insulating layer.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for fabricating a semiconductor device and, more particularly, to a method for forming conductive lines in a semiconductor device in which a trench for forming the upper conductive line is overlapped with contact holes for exposing the lower conductive line, the trench being filled with a conductive metal to form the upper conductive line.

United States Patent **6,586,702**
Wiener-Avnear , et al. **July 1, 2003**

High density pixel array and laser micro-milling method for fabricating array

Abstract

A pixel array device is fabricated by a laser micro-milling method under strict process control conditions. The device has an array of pixels bonded together with an adhesive filling the grooves between adjacent pixels. The array is fabricated by moving a substrate relative to a laser beam of predetermined intensity at a controlled, constant velocity along a predetermined path defining a set of grooves between adjacent pixels so that a predetermined laser flux per unit area is applied to the material, and repeating the movement for a plurality of passes of the laser beam until the grooves are ablated to a desired depth. The substrate is of an ultrasonic transducer material in one example for fabrication of a 2D ultrasonic phase array transducer. A substrate of phosphor material is used to fabricate an X-ray focal plane array detector.

Inventors: **Wiener-Avnear; Eliezer** (Carlsbad, CA); **McFall; James Earl** (Carlsbad, CA)
Assignee: **Laser Electro Optic Application Technology Company** (Carlsbad, CA)
Appl. No.: **780059**
Filed: **February 9, 2001**

Current U.S. Class: **219/121.6**; 219/121.69; 219/121.72
Intern'l Class: B23K 026/00
Field of Search: 219/121.6,121.67,121.68,121.69,121.72 428/209,195

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Primary Examiner: Elve; M. Alexandra
Attorney, Agent or Firm: Brown Martin Haller & McClain, LLP

Goverment Interests

The U.S. Government has rights in this invention pursuant to contract DAMD17-96-C-6032 awarded by the U.S. Department of Defense and contracts NAS9-00008 and NAS9-00119 awarded by NASA under the Small Business Innovation Research (SBIR) Program.

Parent Case Text

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation-In-Part of application Ser. No. 09/557,114 filed Apr. 24, 2000 which was a Continuation of application Ser. No. 09/275,537 filed on Mar. 24, 1999, now U.S. Pat. No. 6,087,618, which was a division of application Ser. No. 08,937,522, filed Sep. 25, 1997, now U.S. Pat. No. 5,956,382.

Claims

We claim:

1. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of a substrate material by application of a predetermined uniform flux per unit area; and

the relative movement of the substrate material and laser beam along each line in said set of lines being repeated until the material has been ablated sufficiently to form a groove of a ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels, each pixel having a first end at said first surface and a second end; and

covering the first ends of the pixels with a layer of acoustic matching material extending over the pixels, whereby the resultant pixel array can transmit and received ultrasonic waves.

2. The method as claimed in claim 1, including the step of adjusting the focus of the laser at periodic intervals after a predetermined number of passes of the laser beam along the groove.

3. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of piezoelectric transducer material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along each line in said set of lines being repeated until the material has been ablated sufficiently to form a groove a ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels; and

filling the grooves with glue material, the glue comprising a flexible epoxy material.

4. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric transducer material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area; and

the relative movement of the substrate material and laser beam along each line in said set of lines being

repeated until the material has been ablated sufficiently to form a groove of ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels.

5. The method as claimed in claim 4, wherein the piezoelectric material is selected from the group consisting of relaxor ferroelectric materials, piezoelectric single crystals, and piezoelectric ceramics.

6. The method as claimed in claim 5, wherein the piezoelectric material is a relaxor ferroelectric material selected from the group consisting of PZN-PT and PMN-PT.

7. The method as claimed in claim 5, wherein the piezoelectric material is a piezoelectric single crystal selected from the group consisting of barium titanate and lithium tantalate.

8. The method as claimed in claim 5, wherein the piezoelectric material is a piezoelectric ceramic comprising a selected composition of lead zirconate titanate (PZT).

9. The method as claimed in claim 1, wherein the relative movement between the laser beam and substrate follows a path along each of the grooves, and then follows the same path repeatedly for a predetermined number of passes until the grooves are ablated to the ***predetermined depth***.

10. The method as claimed in claim 9, wherein the number of passes of the laser beam along each groove is in the range from 10 to 120.

11. The method as claimed in claim 10, wherein the focus of the laser beam is adjusted by 2 to 6 microns after each 10 passes of the laser beam.

12. The method as claimed in claim 1, wherein the laser beam has a Q-switched pulsed output, and the first pulse of the laser output is eliminated prior to application of the laser output to the substrate.

13. The method as claimed in claim 1, including the step of controlling operation of the laser beam in conjunction with the relative movement of the substrate and laser beam such that the laser beam is actuated only when the relative movement is at a constant velocity.

14. The method as claimed in claim 1, wherein the relative movement is a computer-controlled, constant velocity movement along a set of predetermined paths.

15. The method as claimed in claim 14, wherein at least some of the paths are linear.

16. The method as claimed in claim 14, wherein at least some of the paths are curved.

17. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along each line in said set of lines being

repeated until the material has been ablated sufficiently to form a groove of ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels; and

the grid pattern comprising a circular array, with a first set of the grooves being formed in spaced, concentric, circular paths of increasing diameter, and a second set of the grooves comprise a series of spaced lines extending transversely between each adjacent pair of circular grooves.

18. The method as claimed in claim 4, wherein the velocity is in the range from 25 .mu.m/sec to 24.times.10.sup.3 .mu.m/sec.

19. A method of forming an ultrasonic transducer for sending and receiving ultrasonic waves, comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric material, the material having a second surface parallel to said first surface;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along said path being repeated for a predetermined number of passes until the material has been ablated sufficiently to form a groove of predetermined depth;

whereby the grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels, each pixel having a first end at said first surface and a second end at said second surface;

mounting an electrode at the second end of each pixel;

connecting the electrodes to transmitter and receiver electronics; and

encasing the second ends and electrodes in a layer of backing material.

20. The method as claimed in claim 19, including the step of covering the first ends of the pixels with a layer of acoustic matching material extending over the pixels.

Description

BACKGROUND OF THE INVENTION

The present invention is generally concerned with high density pixel array systems, such as imagers, sensors, actuators, detectors and the like, and methods of fabricating such arrays, and is particularly concerned with a method of fabricating a high performance pixel array in exotic materials such as ferroelectric, piezoelectric, pyroelectric, acousto-optic materials and the like for integration in such a system.

United States Patent **6,518,624**
Kim , et al. **February 11, 2003**

Trench-gate power semiconductor device preventing latch-up and method for fabricating the same

Abstract

A trench-gate power semiconductor device and a method for fabricating the same are provided. The trench-gate power semiconductor device includes a semiconductor substrate of a first conductivity type used as a collector region, a buffer layer of a second conductivity type formed on the semiconductor substrate, a drift region of a second conductivity type formed on the buffer layer, a base region of a first conductivity type formed on the drift region, a gate dielectric layer formed on the surface of a trench which is formed down to a predetermined depth into the drift region and surrounds the base region, a gate electrode formed on the gate dielectric layer, an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the base region, an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region, and a collector electrode formed so as to be electrically connected to the semiconductor substrate.

Inventors: **Kim; Hyun-chul** (Shihung, KR); **Yun; Chong-man** (Seoul, KR); **Lee; Kyu-hyun** (Bucheon, KR); **Kim; Ju-il** (Bucheon, KR)

Assignee: **Fairchild Korea Semiconductor Ltd.** (Puchon, KR)

Appl. No.: **734016**

Filed: **December 12, 2000**

Foreign Application Priority Data

May 30, 2000[KR] 00-29298

Current U.S. Class: **257/330**; 257/328; 257/331; 257/401

Intern'l Class: H01L 029/76

Field of Search: 257/328-334,401 438/268-274

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11-87690	Mar., 1999	JP	

Primary Examiner: Loke; Steven
Assistant Examiner: Nadav; Ori
Attorney, Agent or Firm: Rothwell, Figg, Ernst & Manbeck

Claims

What is claimed is:

1. A trench-gate power semiconductor device comprising:

a semiconductor substrate of a first conductivity type used as a collector region;

a buffer layer of a second conductivity type formed on the semiconductor substrate;

a drift region of a second conductivity type formed on the buffer layer;

a base region of a first conductivity type formed on the drift region;

a gate dielectric layer formed on the surface of a trench which is formed down to a ***predetermined depth*** into the drift region and surrounds the base region;

a gate electrode formed on the gate dielectric layer;

an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the base region;

an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region;

a collector electrode formed so as to be electrically connected to the semiconductor substrate; and

a first region of a first conductivity type having a higher impurity concentration than the impurity concentration in the base region, formed so as to be overlapped with a part of the second emitter region in the base region,

wherein the first region of the first conductivity type is a square shape surrounded by the base region, and

each of the corners of the first region of the first conductivity type is extended in a circle shape toward corresponding corners of the trench.

2. The trench-gate power semiconductor device according to claim 1, wherein the base region surrounded by the trench has a square shape.

3. The trench-gate power semiconductor device according to claim 1, wherein the first conductivity type is p-type impurities, and the second conductivity type is n-type impurities.

4. A trench-gate power semiconductor device comprising:

a semiconductor substrate of a first conductivity type used as a collector region;

a buffer layer of a second conductivity type formed on the semiconductor substrate;

a drift region of a second conductivity type formed on the buffer layer;

a base region of a first conductivity type formed on the drift region;

a gate dielectric layer formed on the surface of a trench which is formed down to a ***predetermined depth*** into the drift region and surrounds the base region;

a gate electrode formed on the gate dielectric layer;

an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the base region;

an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region;

a collector electrode formed so as to be electrically connected to the semiconductor substrate; and

a first region of a first conductivity type having a higher impurity concentration than the impurity concentration in the base region, formed so as to be overlapped with a part of the second emitter region in the base region,

wherein the first region of the first conductivity type is a square shape surrounded by the base region, and

two diagonally opposite corners of the first region of the first conductivity type are extended in a circle shape toward corresponding corners of the trench, and the other diagonally opposite corners are extended to one side of the trench and are simultaneously extended to a predetermined length along the sidewall of the trench in the base region, which is arranged along the sidewall of the trench.

5. The trench-gate power semiconductor device according to claim 4, wherein the base region surrounded by the trench has a square shape.

6. The trench-gate power semiconductor device according to claim 4, wherein the first conductivity type is p-type impurities, and the second conductivity type is n-type impurities.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power semiconductor device and a method for fabricating the same, and more particularly, to a trench-gate power semiconductor device preventing latch-up and a method for fabricating the same.

United States Patent **6,511,777**
Pas **January 28, 2003**

Method for manufacturing a phase shift photomask

Abstract

A method for fabricating a phase shift photomask (10) includes providing a photomask (12) having a substantially opaque layer (16) on a surface (14) of a substantially transparent substrate (18). The opaque layer (14) includes a removed portion to define a light transmitting pattern (20) of the photomask (12). The method also includes depositing an implant (22) in a portion of the substrate (18). The implanted portion (24) of the substrate (18) includes an etch rate different than an etch rate of an unimplanted portion (32) of the substrate (18). The method includes initiating an etch of the substrate (18) corresponding to the light transmitting pattern (20) and monitoring a rate of the etch. The method further includes terminating the etch in response to detecting a change in the rate of the etch.

Inventors: **Pas; Sylvia D.** (Plano, TX)
Assignee: **Texas Instruments Incorporated** (Dallas, TX)
Appl. No.: **666933**
Filed: **September 21, 2000**

Current U.S. Class: **430/5**; 216/62
Intern'l Class: G03F 009/00; C03C 015/00
Field of Search: 430/5,322,323,30 216/62,87

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Primary Examiner: Rosasco; S.
Attorney, Agent or Firm: Keagy; Rose Alyssa, Brady, III; W. James, Telecky, Jr.; Frederick J.

Parent Case Text

This application claims priority under 35 USC .sctn.119(e)(1) of provisional application No. 60/163,864 filed Nov. 5, 1999.

Claims

What is claimed is:

1. A method for fabricating a phase shift photo mask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

depositing an implant in a portion of the substrate, the implanted portion of the substrate having an etch rate different than an etch rate of an unimplanted portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch; and

terminating the etch in response to detecting a change in the rate of the etch.

2. The method of claim 1, wherein depositing the implant comprises implanting a dopant to a ***predetermined depth*** of the substrate from the surface of the substrate.

3. The method of claim 2, wherein terminating the etch comprises terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate.

4. The method of claim 1, wherein depositing the implant comprises implanting an interlayer at a ***predetermined depth*** of the substrate from the surface of the substrate.

5. The method of claim 4, further comprising:

monitoring the etch to detect the etch rate of the unimplanted portion of the substrate;

monitoring the rate of the etch to detect an etch rate of the interlayer; and

wherein terminating the etch comprises terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate after detecting the etch rate of the interlayer.

6. The method of claim 1, wherein depositing the implant comprises:

implanting a dopant to a ***predetermined depth*** of the substrate from the surface of the substrate, wherein the etch rate of the implanted portion of the substrate is greater than the etch rate of the unimplanted portion of the substrate; and

wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the implanted portion of the substrate.

7. The method of claim 1, wherein depositing the implant comprises implanting an interlayer in the substrate, the interlayer disposed a predetermined distance from the surface of the substrate, the interlayer having a substantially uniform thickness, and wherein terminating the etch comprises terminating the etch in response to detecting a change in the rate of the etch corresponding to the etch rate of the unimplanted portion of the substrate after

detecting an etch rate of the interl.., er.

8. A method for fabricating a phase shift photomask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

implanting a dopant into a portion of the substrate corresponding to the light transmitting pattern, the doped portion of the substrate having an etch rate different than an etch rate of the undoped portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch; and

terminating the etch in response to detecting the etch rate of the undoped portion of the substrate.

9. The method of claim 8, wherein implanting the dopant comprises implanting the dopant to a ***predetermined depth*** of the substrate, the ***predetermined depth*** corresponding to a desired light phase shift.

10. The method of claim 8, wherein the etch rate of the doped portion of the substrate is greater than the etch rate of the undoped portion of the substrate, and wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the doped portion.

11. The method of claim 8, wherein implanting the dopant comprises implanting the dopant to a substantially uniform depth of the substrate, the depth corresponding to a desired light phase shift.

12. The method of claim 8, wherein the etch comprises a wet etch.

13. The method of claim 8, wherein monitoring the rate of the etch comprises:

detecting the etch rate of the doped portion of the substrate; and

detecting the etch rate of the undoped portion of the substrate after detecting the etch rate of the doped portion.

14. A method for fabricating a phase shift photomask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

implanting an interlayer in a portion of the substrate, the implanted portion of the substrate having an etch rate different than an etch rate of an unimplanted portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch;

detecting the etch rate of the implanted portion of the substrate; and

terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate after detecting the etch rate of the implanted portion.

15. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer at a ***predetermined depth*** of the substrate, the ***predetermined depth*** corresponding to a desired light phase shift.

16. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer in the substrate, the interlayer having a substantially uniform thickness.

17. The method of claim 14, wherein the etch rate of the implanted portion of the substrate is greater than the etch rate of the unimplanted portion of the substrate, and wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the implanted portion.

18. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer in the portion of the substrate corresponding to the light transmitting pattern.

19. The method of claim 14, wherein initiating the etch comprises initiating a dry etch.

20. The method of claim 14, wherein monitoring the rate of the etch further comprises detecting the etch rate of the unimplanted portion of the substrate prior to detecting the etch rate of the implanted portion of the substrate.

Description

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of wafer manufacturing and, more particularly, to a method for manufacturing a phase shift photomask.

BACKGROUND OF THE INVENTION

Significant advancements in the miniaturization of semiconductor integrated circuits have been made in recent years. With such advancements, a reduction in a size of circuit patterns formed on semiconductor substrates, or wafers, has been achieved. One technique for producing a circuit pattern on a wafer includes photolithography. The photolithography technique generally includes transferring a circuit pattern from a photomask onto the wafer. The photomask is generally constructed by depositing a substantially opaque layer of material on a surface of a substantially transparent substrate. Portions of the opaque layer are then removed to form the pattern to be transferred to the wafer during a light exposure step of the photolithography process.

A photomask may also be used to provide phase shifting in the photolithography process. Phase shifting generally creates positive and negative phase light interference when administering the light exposure step in the photolithography process. Exposure light reaching an unexposed region of the wafer due to optical diffraction is generally canceled out by light reaching the exposed regions of the wafer because the light transmitted through the phase shift portion of the photomask is opposite in phase. Thus, phase shifting generally provides increased resolution of transferred patterns projected onto the wafer.

Forming a photomask for use with phase shift photolithography processing generally requires reducing a thickness of the light transmitting portion of the photomask substrate to produce a desired light phase shift. Reducing the thickness of the light transmitting portion of the photomask substrate may be accomplished by etching or other suitable processes. For example, the light transmitting portion of the photomask substrate may be chemically etched until a desired thickness of the photomask substrate is obtained to produce the desired light phase shift.

However, prior methods for manufacturing a phase shift photomask suffer several disadvantages. For example, variations in etching operations generally result in imprecise thicknesses of the light transmitting portions of the photomask substrate. For example, variations in the time, temperature, RF power, and other etch process variables are generally difficult to monitor and control. Thus, the resulting light phase shift often varies from the desired light phase shift due to a deviation between the obtained photomask substrate thickness and the desired photomask substrate thickness.

SUMMARY OF THE INVENTION

United States Patent **6,225,234**
Miller , et al. **May 1, 2001**

In situ and ex situ hardmask process for STI with oxide collar application

Abstract

A method or process for etching a trench in an IC structure is disclosed. The IC structure might be comprised of a plurality of different component materials arranged proximate to one another, all of which need to be etched down to a target level. A first etching chemistry is applied which preferentially etches a one type of component material. A second etching chemistry is applied which preferentially etches another type of component material. The method or process toggles back and forth between the etching chemistries until the target level is reached. The toggling techniques serves to maintain the profiles of the different component materials. One component material might also be embedded, as a collar or otherwise, around another component material. The toggling technique can serve to modulate the height, level, or shape of one material relative to another material. The toggling steps can be performed in situ or ex situ. The toggling technique can be used with different mask materials, including a photoresist or a hardmask over the IC structure.

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Current U.S. Class: **438/734**; 438/735; 438/737; 438/738
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Field of Search: 438/734,735,737,738

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Primary Examiner: Dang; Trung
Attorney, Agent or Firm: Beyer Weaver & Thomas, LLP

Claims

What is claimed is:

1. A method for etching a portion of an integrated circuit (IC) structure down to a certain ***target depth,*** the structure having a first component material area, and at least a second component material area arranged proximate to the first component material area, the method comprising:

(i) applying a first type of etching chemistry which preferentially etches the first component material area;

(ii) applying a second type of etching chemistry which preferentially etches the second component material area; and

repeating steps (i) and (ii) until the certain ***target depth*** is achieved, wherein certain profiles of the IC structure and its component material areas are maintained by toggling back and forth between the etching chemistries.

2. The method of claim 1, wherein etching a portion of an IC structure includes the formation of shallow trench isolation (STI) features.

3. The method of claim 1, wherein the first type of etching chemistry and second type of etching chemistry are applied in situ.

4. The method of claim 1, wherein the second component material area is embedded within the first component material area.

5. The method of claim 4, wherein a portion of the second component material area is modulated in height relative to the first component material area via toggling back and forth between the etching chemistries.

6. The method of claim 5, wherein the IC structure is a memory device, with the first component material area including at least a poly-silicon portion of material and a crystalline silicon portion of material and the second component material area including at least silicon oxide material.

7. The method of claim 5, wherein the memory device is a DRAM having deep trench capacitors.

8. The method of claim 6, wherein the second component material area is in the shape of a collar surrounding the poly-silicon material portion of material, whereby the toggling back and forth between the etching chemistries maintains the profile of the collar.

9. The method of claim 1, wherein the first type of etching chemistry preferentially etches crystalline or amorphous silicon materials.

10. The method of claim 9, wherein the materials include poly and single crystalline silicon materials.

11. The method of claim 10, wherein the first type of etching chemistry includes a mixture of Cl2 and HBr.

12. The method of claim 11, wherein the preferred ratio of Cl2-to-HBr is approximately 1-to-3.

13. The method of claim 9, wherein the second type of etching chemistry preferentially etches oxide materials.

14. The method of claim 13, wherein the second type of chemistry includes a mixture of CF4 and CHF3.

15. The method of claim 14, wherein the preferred ratio of CF4-to-CHF3 is approximately 3-to-1.

16. The method of claim 1, wherein the etching steps are used in association with a photoresist mask over at least a portion of the IC structure.

17. The method of claim 1, wherein the etching steps are used in association with a hard mask over at least a portion of the IC structure.

18. A process for etching to a target level a portion of an integrated circuit (IC) structure comprised of a plurality of different types of component materials, the process comprising:

(i) applying an etching chemistry to preferentially etch certain types of the plurality of component materials;

(ii) applying an etching chemistry to preferentially etch certain remaining other types of the plurality of component materials;

repeating steps (i) and (ii) until the target level is achieved, wherein certain profiles of the IC structure and its component material areas are maintained by toggling back and forth between the etching chemistries.

19. The process of claim 18, wherein the process of etching to a target level a portion of an IC structure includes the formation of shallow trench isolation (STI) features.

20. The process of claim 18, wherein different etching chemistries are applied in situ.

21. The process of claim 19, wherein one type of component material is embedded within another type of component material.

22. The process of claim 17, wherein one type of component material is modulated in height relative to another type of component material via toggling back and forth between the etching chemistries.

23. The process of claim 22, wherein the IC structure is a memory device with a first type of component material including at least a poly-silicon portion of material and a crystalline silicon portion of material and a second type of component material area including at least silicon oxide material.

24. The process of claim 23, wherein the memory device is a DRAM having deep trench capacitors.

25. The process of claim 23, wherein the second type of component material is in the shape of a collar surrounding the poly-silicon material portion of material, whereby the toggling back and forth between the etching chemistries maintains the profile of the collar.

26. The process of claim 18, wherein the etching chemistry in step (i) preferentially etches crystalline or amorphous silicon materials.

27. The process of claim 26, wherein the materials include poly and single crystalline silicon materials.

28. The process of claim 26, wherein the etching chemistry in step (i) includes a mixture of Cl2 and HBr.

29. The process of claim 28, wherein the preferred ratio of C12-to-HBr is approximately 1-to-3.

30. The process of claim 26, wherein the etching chemistry in step (ii) preferentially etches oxide materials.

31. The process of claim 30, wherein the etching chemistry in step (ii) includes a mixture of CF4 and CHF3.

32. The process of claim 31, wherein the preferred ratio of CF4-to-CHF3 is approximately 3-to-1.

33. The method of claim 18, wherein the etching steps are used in association with a photoresist mask over at least a portion of the IC structure.

34. The method of claim 18, wherein the etching steps are used in association with a hard mask over at least a portion of the IC structure.

Description

BACKGROUND OF THE INVENTION

The present invention relates to the fabrication of semiconductor integrated circuits (IC's). More particularly, the present invention relates to a process or method for controlled etching through an IC structure which has two or more materials arranged together, and where the height of one of the materials may need to be modulated relative to the other materials.

During the manufacture of a semiconductor-based product, for example, a flat panel display or an integrated circuit such as a memory cell, multiple deposition and/or etching steps may be employed. By way of example, one method of etching is plasma etching. In plasma etching, a plasma is formed from the ionization and dissociation of process gases. The positively charged ions are accelerated towards the substrate where they, in combination with neutral species, drive the etching reactions. In this manner, etched features such as vias, contacts, or trenches may be formed in the layers of the substrate.

Recently, shallow trench isolation (STI) has grown in popularity as a preferred method for forming a trench that can, among other applications, electrically isolate individual transistors in an integrated circuit. Electrical isolation is needed to prevent current leakage between two adjacent devices (e.g., transistors). Broadly speaking, conventional methods of producing a shallow trench isolation feature include: forming a hard mask over the targeted trench layer, patterning a soft mask over the hard mask, etching the hard mask through the soft mask to form a patterned hard mask, and thereafter etching the targeted trench layer to form the shallow trench isolation feature. Subsequently, the soft mask is removed (e.g., stripped) and the shallow trench isolation feature is back-filled with a dielectric material.

FIGS. 1A-1C are cross sectional views of the conventional process steps that maybe used to form shallow trench isolation features. Referring initially to FIG. 1A, there is shown a typical layer stack 10 that is part of a substrate or semiconductor wafer (not drawn to scale for ease of illustration). A silicon layer 12 is located at the bottom of layer stack 10. A pad oxide layer 14 is formed above silicon layer 12 and a nitride layer 16 is formed above pad oxide layer 14. In most situations, the pad oxide layer is used as the interlayer that is disposed between the nitride layer and the silicon layer. Furthermore, in order to create a patterned hard mask with pad oxide layer 14 and nitride layer 16, a photoresist layer 18 is deposited and patterned using a conventional photolithography step over nitride layer 16. After patterning, soft mask openings 20 (narrow) and 22 (wide) are created in photoresist layer 18 to facilitate subsequent etching. The above-described layers and features, as well as the processes involved in their creation, are well known to those skilled in the art.

Following the formation of layer stack 10, nitride layer 16 and pad oxide 14 are subsequently etched to create a hard mask, which includes a narrow hard mask opening 24 and a wide hard mask opening 26, as seen in FIG. 1B. The hard mask openings are used to pattern the trench during etching of the silicon layer. For the most part, etching stops after reaching silicon layer 12, however, a small portion 28 on the surface of silicon layer 12 is typically etched away during the etching of pad oxide layer 14. Moreover, a gas chemistry that includes CF4 is generally used to facilitate etching through the nitride and pad oxide layers. Typically, the CF4 chemistry etches the side walls of nitride layer 16, pad oxide layer 14 and small portion 28 of silicon layer 12 anisotropically (i.e., substantially straight down).

Once hard mask openings are created through nitride layer 16 and pad oxide layer 14, silicon layer 12 is etched therethrough to form shallow trench isolation features, for example, a narrow feature 30 and a wide feature 32, as

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Patent Attorney Docket No. MTI-31267

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant (s)	:	Polinsky et al.
Serial No.	:	09/584,975
For	:	Modified Facet Etch to Prevent Blown Gate Oxide and Increase Chamber Life
Filed	:	May 14, 2001
Examiner	:	Lynette T. Umez Eronini
Group Art Unit	:	1765
Confirmation No.	:	0989

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

I hereby certify that, on the date shown below, this correspondence is being:

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■ transmitted by facsimile to Fax No.: 1-703-872-9310 addressed to Examiner L. T. Umez Eronini at the Patent and Trademark Office.

Date: February 24, 2003 Rose Story

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

RESPONSE UNDER 37 C.F.R. § 1.111

This response replies to the Office Action mailed February 4, 2003 (Paper No. 3).

The Examiner rejected Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. § 112, second